120GHz Imaging Sensor

DESIGN DOCUMENT

Team 40

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Executive Summary

Development Standards & Practices Used

List all standard circuits, hardware, software practices used in this project. List all the Engineering standards that apply to this project that were considered.

USB 2.0

Summary of Requirements

List all requirements as bullet points in brief.

- Design RF circuit that contains radar IC and phased-lock-loop (PLL) circuitry.
- Design data acquisition (including amplifier, low pass filter, and ADC) and control circuitry with FPGA.
- Program FPGA to interface to ADCs for data collection from RF circuit.
- Program a USB chip to interface to a PC for data transfer.
- Program a GUI on the PC to interface to the FPGA.
- Conduct radar imaging experiments in the microwave lab at CNDE.

Applicable Courses from Iowa State University Curriculum

List all Iowa State University courses whose contents were applicable to your project.

- CPRE 281: Digital Logic
- EE 230: Electronics Circuit and System
- EE 414/ 514: Microwave Engineering
- EE 311: Electromagnetics
- EE 411: Wave Propagation and Transmission Lines
- EE 333: Electronic System Design

New Skills/Knowledge acquired that was not taught in courses.

List all new skills/knowledge that your team acquired which was not part of your Iowa State curriculum in order to complete this project.

FPGA programming, Custom USB data transfer

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1 Team, Problem Statement, Requirements, and Engineering Standards

1.1 Team Members

Huyen Vy Pham

Aaron McCarville

Gunnar Hageman

Noah Gaffney

Benjamin Podjenski

1.2 Required Skill Sets for Your Project

(if feasible – tie them to the requirements)

Requirements include PCB design, design simulation for making the Radar IC board and data acquisition board. FPGA and embedded programming skills are needed to configure/ program the FPGA to collect RF data from the data acquisition board. Software design is needed to build a user interface application for interfacing the FPGA and computer.

1.3 Skill Sets covered by the Team

(for each skill, state which team member(s) cover it)

Huyen Vy Pham: PCB design, C, MATLAB, Python, RF measurement

Aaron McCarville: Xilinx FPGA's, USB, KiCad, Python, C, C++, RF measurement

Noah Gaffney: KiCad, C, PCB design, circuit assembly

Gunnar Hageman: Python, C, Java, Armature Radio background, project management/design doc work

Benjamin Podjenski: Java, C, Python, .NET, systems engineering experience.

1.4 Project Management Style Adopted by the team

We decided to use transformational management style. With this style, we focus mainly on setting goals/ issues and milestones for the projects. Everyone is responsible for a part of the project. Each person will present the work at weekly meetings and other team members can provide feedback or help if the issue owner needs. In addition, each team member can ask for help working on the project. Communication in the team should be maintained and frequent.

1.5 Initial Project Management Roles

(Enumerate which team member plays what role)

Huyen Vy Pham: Team leader – maintaining the git issue board and communicating with advisor.

Aaron McCarville: Lead hardware design.

Noah Gaffney: Hardware design and testing.

Gunnar Hageman: Embedded programming

Benjamin Podjenski: Software programming for GUI

1.6 Problem Statement

What problem is your project trying to solve? Use non-technical jargon as much as possible.

We are building a 120 GHz millimeter wave (mm-wave) imaging radar. The radar is used to detect objects from a distance. The radar board will be then used to conduct imaging in the Center for Nondestructive Evaluation.

1.7 Requirements & Constraints

*List all requirements for your project. This includes functional requirements (specification), resource requirements, qualitative aesthetics requirements, economic/market requirements, environmental requirements, UI requirements, performance requirements, legal requirements, maintainability requirements, testing requirements and any others relevant to your project. When a requirement is also a quantitative constraint, either separate it into a list of constraints, or annotate at the end of requirement as "**(constraint)**". Other requirements can be a single list or can be broken out into multiple lists based on the category.*

a) Functional requirements:

- The system includes two sub-systems: Radio Frequency Board (includes the Radar IC and the PLL circuitry), the data acquisition board (includes a filter, an amplifier, and an ADC), and a FPGA.
- The Radio Frequency Board should emit the frequency at 120GHz. The functionality is tested by spectrum analyzer. The tunning time for the board is required to be 5ms and is desired to be 1ms.
- The data acquisition board should be able to process data at the rate of roughly around 1000 samples per 1ms.
- The FPGA is used to perform data analysis and control the Radar IC and PLL IC.
- The USB is used to interface between the FPGA and the PC.

b) UI requirements:

- The GUI on the PC should be able to send the control parameters to program Radar IC, and PLL IC. The GUI should also be able to check the status of those ICs. Users can use the GUI to know targets that have been detected and at which distance.

c) Testing requirements:

- The spectrum analyzer should be used to check the performance of the Radio Frequency Board and to know the tunning time.

- The Radar Board will be used to do image scanning in the Center for Nondestructive Evaluation. The image result should show the defects/ holes inside the object.

d) Qualitative aesthetics requirements:

- The size of the board should be 8x5x5 cm. The board should be small enough to be mounted on the scanner in the Center for Nondestructive Evaluation.

1.8 ENGINEERING STANDARDS

What Engineering standards are likely to apply to your project? Some standards might be built into your requirements (Use 802.11 ac Wi-Fi standard) and many others might fall out of design. For each standard listed, also provide a brief justification.

- USB 2.0: USB is an interface that connects a device to a computer. With this connection, the computer sends or retrieves data from the device. USB 2.0 was released in April 2000, adding a higher maximum signaling rate of 480 Mbit/s (maximum theoretical data throughput 53 Mega Byte/s) named High Speed or High Bandwidth, in addition to the USB 1.x. The USB standard is applied to interface between the FPGA and the computer.
- Verilog IEEE 1364: is a hardware description language (HDL) used to model electronic systems. It is most used in the design and verification of digital circuits at the register-transfer level of abstraction. The standard is applied when programming the FPGA.
- IEEE Standard for Electrical Characterization of Printed Circuit Board and Related Interconnects at Frequencies up to 50GHz. IEE 370-2020: This standard addresses the quality of measured S-parameters for electrical printed circuit board (PCB) and related interconnect at frequencies up to 50 GHz. This standard is applied for RF subsystem PCB design and test.
- BM SAA - a set of software interfaces, conventions, and protocols that provide a framework for designing and developing applications: The standard is used for software development of GUI. The standard is used to ensure the application programs look and work in the same manner while being designed by multiple people.

1.9 INTENDED USERS AND USES

Who benefits from the results of your project? Who cares that it exists? How will they use it? Enumerating as many "use cases" as possible also helps you make sure that your requirements are complete (each use case may give rise to its own set of requirements).

- Intended Users: Millimeter wave lab in the Center for Nondestructive Evaluation and its business partners.
- Uses: To be used to detect objects at a distance, and to conduct imaging to detect defects/ holes/ cracks in the sample.

2 Project Plan

2.1 TASK DECOMPOSITION

In order to solve the problem at hand, it helps to decompose it into multiple tasks and subtasks and to understand interdependence among tasks. This step might be useful even if you adopt agile *methodology. If you are agile, you can also provide a linear progression of completed requirements aligned with your sprints for the entire project. At minimum, this section should have a task dependence graph, description of each task, and a justification of your tasks with respect to your requirements. You may optionally also include sub-tasks.*

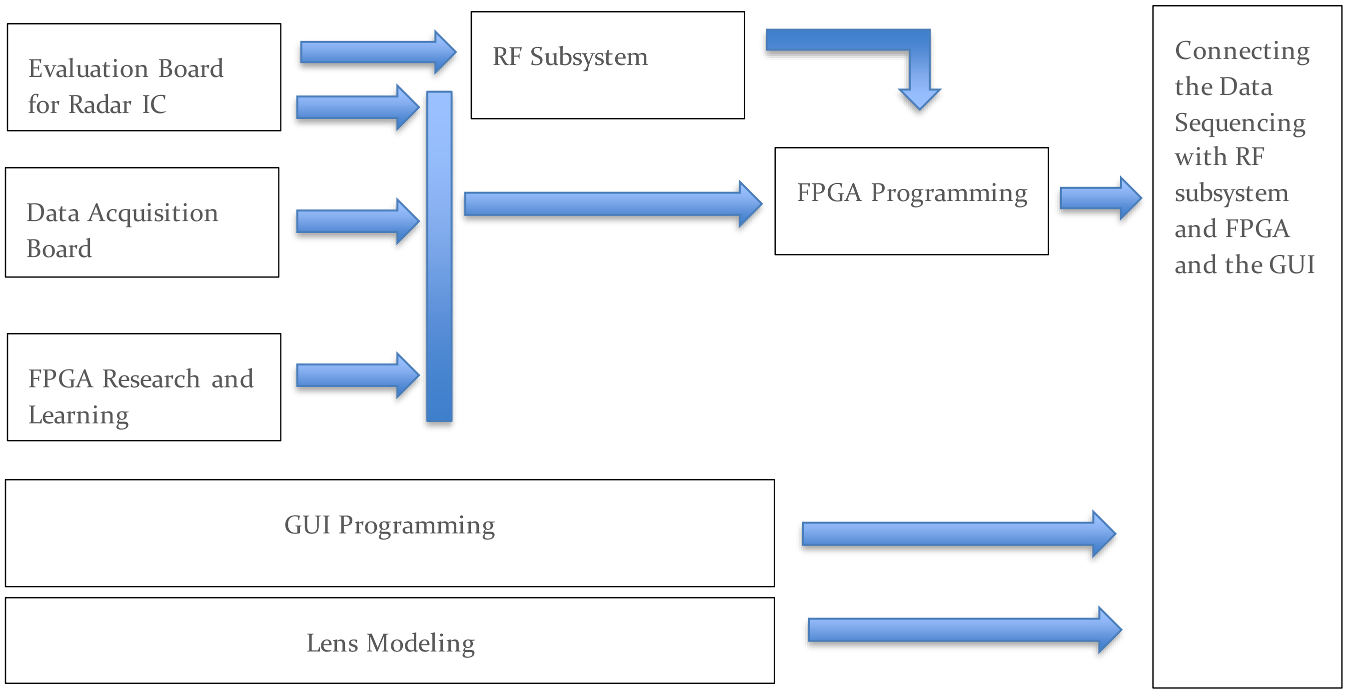

Figure 1: Task Decomposition Diagram

Tasks in details:

a) Evaluation Board for Radar IC: The evaluation board contains a Phase Lock Loop IC and a Phase Lock Loop circuitry, and the Radar IC. The purpose of the board is to understand the outputs (IFI and IFQ) and the frequency lock time of the recommended circuitry for Phase Lock Loop to improve the design.

Subtask:

- Make Schematic for Evaluation Board (based on the TRA120_045's Evaluation Board Schematic)
- Do Layout for Evaluation Board
- Evaluation Board Review
- Evaluation Board Testing

b) Data Acquisition Board: The Data Acquisition contains a filter, a controllable amplifier, and an ADC. The board is connected to the RF board (or the IC Radar Evaluation Board) to get IFI and IFQ data and converts from analog signal to discrete time and discrete amplitude digital signal. Those data will then be transferred to the FPGA for processing.

The Data Acquisition Board can be made and tested separately from the RF board (or the IC Radar Evaluation Board).

Subtask:

- Research on different ADCs based on sampling rate and resolution. The desired value for sampling rate is 1MHz, and for resolution is 12-16 bit. The SNR (signal to noise ratio) should be high to cope with noise. The desired ADC should have differential inputs. The desired logic voltage level is 3.3V or 5V, following the FPGA logic voltage level.

- Research on amplifiers. The desired requirement is that the amplifier has differential inputs and outputs.

- Research on filters.

- Make a schematic for the Data Acquisition Board

- Do the layout for the Data Acquisition Board

- Test the Data Acquisition Board

c) Learning the FPGA programing: The big task includes the research on Alchitry Board and learning Vivado and Vitis for programming the FPGA. The FPGA has three main functionalities: receiving data from the Data Acquisition Board, communicating through SPI to the RF board and the ADC, and interfacing with PC.

Subtask:

- Research the Alchitry Board, including pin assignments.

- Learning Vivado

- Learning Vitis

- Make a small program for the board like turning on and off the LED.

d) Programing the FPGA: to receive data from the Data Acquisition Board, communicate through SPI to the RF board and the ADC, and interface with PC.

Subtask:

- Program the FPGA to receive data from the Data Acquisition Board

- Program the FPGA to communicate with the RF board and the Data Acquisition Board through SPI

- Program the FPGA to interface with PC using the FTDI cables.

e) RF subsystem: The board contains a Phase Lock Loop IC and a Phase Lock Loop circuitry, and the Radar IC. The board uses the any changes in design from the evaluation board to make the actual RF subsystem.

Subtask:

- Design a new PLL circuitry.

- Simulate the PLL circuitry for bandwidth and locked time understanding.

- Make Schematic for RF subsystem.

- Do Layout for RF board.

- RF Board Review

- RF Board Testing

f) Making the GUI for User Interface: The application can be standalone application or local host website that receives the data from the FPGA and do data processing. The app illustrates the data using a graph with different options. In addition, the users can also control the whole system from the app, such as providing start and stop frequency or provide signal to start or stop capturing the data.

Subtask:

- Making the front-end of the application

- Making the back-ends of the application that does not needs to interface with the FPGA, including data illustration with different options and data processing the received data

- Making the back-ends of the application to interface with the FPGA, including receiving the data from the FPGA, sending control signals to the FPGA

- Connecting the front-end and the back end of the application.

- Testing

g) Lens Modeling: The activity is to understand the radar chip on board and how the far field signal looks like. The activity can also help to improve the radar path by remaking the lens if needed.

Subtask:

- Model the lens using the CST application with the antenna modeled from the radar information on the datasheet.

h) Connecting the Data Sequencing with RF subsystem and FPGA and the GUI: Test the final product.

2.2 PROJECT MANAGEMENT/TRACKING PROCEDURES

Which of agile, waterfall or waterfall+agile project management style is you adopting? Justify it with respect to the project goals.

What will your group use to track progress throughout the course of this and the next semester. This could include Git, GitHub, Trello, Slack or any other tools helpful in project management.

Our group plans to use a hybrid of waterfall and agile project management style, as it fits best with our project goals. There are certain stages of our projects that need to be completed prior to other stages. For example, our RF subsystem and Data Acquisition subsystem need to be completed prior to FPGA programming. This example illustrates the use of waterfall model. On the other hand, the RF subsystem and the Data Acquisition subsystem can be worked in parallel, which is one of the benefits of agile project management style.

To track our project progress, we utilize different resources as shown below:

- Microsoft Team: We use MS Team daily for progress tracking and collaboration. It is the primary communication tool besides weekly meetings.

- Microsoft Calendar: We use Microsoft Calendar to schedule meetings. In the future, we are going to the calendar for important reminders, such as milestones or hard deadlines.

- CyBox: Cybox is home for our documents, such as design documents or weekly, bi-weekly reports. It will soon host documents, such as Bill of Material, Design files, etc.

- GitLab: We use the Gitlab project management features to put Milestones and track issues

2.3 Project Proposed Milestones, Metrics, and Evaluation Criteria

What are some key milestones in your proposed project? It may be helpful to develop these milestones for each task and subtask from 2.1. How do you measure progress on a given task? These metrics, preferably quantifiable, should be developed for each task. The milestones should be stated in terms of these metrics: Machine learning algorithm XYZ will classify with 80% accuracy; the pattern recognition logic on FPGA will recognize a pattern every 1 ms (at 1K patterns/sec throughput). ML accuracy target might go up to 90% from 80%.

In an agile development process, these milestones can be refined with successive iterations/sprints (perhaps a subset of your requirements applicable to those sprint).

a) Milestone 1: Evaluation Board Design and Test

Metrics and Evaluation Criteria:

- Functional:

+ Read IFI and IFQ using an ADC while sweeping the frequency using an FTDI cable. The data should be read via FTDI cable. The data should then be processed using the IFFT to gain understanding of the change of I + j*Q data (magnitude) versus distance. The data should show the distance at which the known target is displayed.

+ Using the spectrum analyzer to check the frequency locked at 120GHz and to determine lock time (or the lock time can be determined by accessing the register of Phase-Lock-Loop IC). The lock time should be less than 5ms. The locked frequency should be 120GHz.

b) Milestone 2: Data Acquisition Board

Metrics and Evaluation Criteria:

- The chosen ADC should satisfy the desired requirements: the sampling rate is 1Mhz, the logic voltage level is 3.3V, and the input is differential pairs. The ADC should have 2 channels built in. If satisfying 3/4 requirements, it is a good ADC.

- For testing, when ADC is supplied with a voltage signal, we should be able to read back the data using the Alchitry.

c) Milestone 3: GUI

Metrics and Evaluation Criteria:

- GUI should have options for displaying and options for controls on the interface.

- GUI should be able to communicate with the FPGA and control the system based on the user's choice: start/ stop frequency, start/ stop signal to capture data, etc.

- GUI should be able to display the IFI and IFQ data in different forms (magnitude, phase, Raw data).

d) Milestone 4: Lens Modeling

Metrics and Evaluation Criteria:

- The lens is modelled in the CST using the information on the antenna on chip provided by the manufacturer. The far field is shown with direction.

e) Milestone 5: FPGA programming

Metrics and Evaluation Criteria:

- FPGA can send commands over SPI to Acquisition Board and RF Board.

- FPGA can sample the ADC data via SPI

- FPGA can send data to Host computer.

2.4 Project Timeline/Schedule

• A realistic, well-planned schedule is an essential component of every well-planned project

• Most scheduling errors occur as the result of either not properly identifying all of the necessary activities (tasks and/or subtasks) or not properly estimating the amount of effort required to correctly complete the activity

• A detailed schedule is needed as a part of the plan:

– Start with a Gantt chart showing the tasks (that you developed in 2.2) and associated subtasks versus the proposed project calendar. The Gantt chart shall be referenced and summarized in the text.

– Annotate the Gantt chart with when each project deliverable will be delivered

• Project schedule/Gantt chart can be adapted to Agile or Waterfall development model. For agile, a sprint schedule with specific technical milestones/requirements/targets will work.

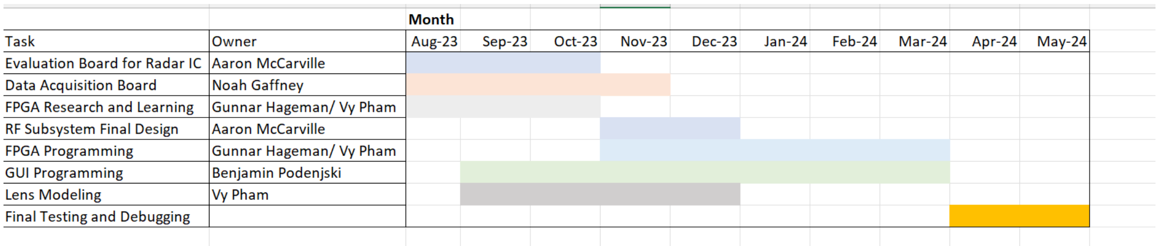

Figure 2: Project Schedule

2.5 Risks And Risk Management/Mitigation

Consider for each task what risks exist (certain performance target may not be met; certain tool may not work as expected) and assign an educated guess of probability for that risk. For any risk factor with a probability exceeding 0.5, develop a risk mitigation plan. Can you eliminate that task and add another task or set of tasks that might cost more? Can you buy something off-the-shelf from the market to achieve that functionality? Can you try an alternative tool, technology, algorithm, or board?

Agile projects can associate risks and risk mitigation with each sprint.

Table 1: Risk and Risk Management

Risk	Alternative
Data Acquisition Board doesn't work	Using the ADC built-in in the FPGA
USB doesn't work	Using FTDI come with the Alchitry
New Lense doesn't work	Using the provided lens

2.6 Personnel Effort Requirements

Include a detailed estimate in the form of a table accompanied by a textual reference and explanation. This estimate shall be done on a task-by-task basis and should be the projected effort in total number of person-hours required to perform the task.

Table 2: Personnel Effort Requirements

Task	Person – hrs/week	#of weeks	Total
Evaluation Board for Radar IC	10	10	100
RF subsystem Design and Test	10	10	100
Data Acquisition Board	12	10	120
Learning the FPGA programing	10	10	100
Programing the FPGA	15	10	150
Making the GUI for User Interface	10	20	200

Lens Modeling	5	5	25
Final Product and Testing	20	5	50
Document	5	20	100
Total			945

2.7 Other Resource Requirements

Identify the other resources aside from financial (such as parts and materials) required to complete the project.

Material and parts that are required to complete the project:

- Alchitry FPGA.
- Radar IC TRA120_045.
- Components for Data Acquisition Board and RF Board.

4 Design

4.1 Design Content

Briefly describe what is the design content in your project.

For our project we are designing a fully functional computer-controlled radar system, this system is broken down into several individually designed parts. A focusing lens, A PLL for the radar chip control, a secondary board with ADCs and filters for gathering data from the Radar chips itself, an FPGA board to link all the hardware components to a web App via a raspberry pi.

4.2 Design Complexity

Provide evidence that your project is of sufficient technical complexity. Use the following metric or argue for one of your own. Justify your statements (e.g., list the components/subsystems and describe the applicable scientific, mathematical, or engineering principles)

1. *The design consists of multiple components/subsystems that each utilize distinct scientific, mathematical, or engineering principles.*
2. *The problem scope contains multiple challenging requirements that match or exceed current solutions or industry standards.*

Our design contains multiple components and subsystems that each require different engineering skills, such as circuit design, embedded programming, and software programming. Furthermore, the scope of the problem we seek to solve contains multiple challenging requirements that match or exceed current solutions and industry standards. A list of subsystems and actions:

a) RF PCB Design (Phase Lock Loop with Radar IC): Complex circuit design, signal reception and processing, circuit board customization, data transfer.
b) ADC PCB Design: Programming the ADC configuration and data acquisition.

c) FPGA Embedded Programming: Programming the FPGA for data processing from the ADC board, and for communicating through SPI with ADC and the PLL chip. The programming is done through Xilinx platform.
d) GUI Programming: The GUI interface is used for data processing, signal control, and data display, which is programmed in Python. GUI is a website and is hosted on a Raspberry Pi.
e) Lens Modeling and Measurement: The lens modeling is done through CST to understand the far field pattern using information (shape/ dimension) of the on-chip antenna.

4.3 Modern Engineering Tools

What modern engineering tools were used for this design? Their roles.

a) GUI software: For the role of the software on the PC we are using a web application framework Django to create the GUI for the system. This is to control the radar and display the output in a logical manner. To interact with the front-end GUI, we are hosting the web application on a Raspberry Pi using an Apache webserver.
b) Embedded Programming: Xilinx platform, Vivado (Hardware) and Vitis (Software) will be used to program the FPGA, and FTDI will be used to communicate commands from the PC to the FPGA as well as return the filtered data to the PC for display.
c) Lens Modeling: CST software is used to model the lens and antenna on chips. Spectrum Analyzer is used to measure the patterns.
d) RF and ADC board: KiCad is used to make the schematic and layout.

4.4 Design Context

Describe the broader context in which your design problem is situated. What communities are you designing for? What communities are affected by your design? What societal needs does your project address?

List relevant considerations related to your project in each of the following areas:

Area	Description	Examples
Public health, safety, and welfare	The scope includes the construction profession, the electrician profession, the craftsman profession, and the health care profession. We provide them with a tool that will ensure they are performing safe, well-informed work.	This will help detect different objects and the structure of the objects. This will help inform people from those areas.
Global, cultural, and social	There are several applications of the product, such as healthcare, construction, etc. Those professions take up a big portion in the area. Thus, the project will have a bigger impact.	The development would not violate any ethics code or become harmful to global, cultural, and social activities. The development might transform the way people do things, like doing nondestructive testing or medical testing.

Environmental	Our product design does not require regular consumption of environmentally harmful goods. The components used in the product design and manufacture, however, may include plastics and precious metals	There are no impacts or changes to the environment, as our products does not violate any environmental requirements.
Economic	Our product should help with detecting objects that might cause harm to workers in the field. This helps with safety costs. In addition, the product should be very cost friendly and affordable to wide range of users.	The product's cost is very affordable and can be used for many applications.

4.5 Prior Work/Solutions

Include relevant background/literature review for the project.

– If similar products exist in the market, describe what has already been done

*– If you are following previous work, cite that and discuss the **advantages/shortcomings***

– Note that while you are not expected to "compete" with other existing products / research groups, you should be able to differentiate your project from what is available. Thus, provide a list of pros and cons of your target solution compared to all other related products/systems.

Detail any similar products or research done on this topic previously. Please cite your sources and include them in your references. All figures must be captioned and referenced in your text.

There are some similar products. They are all well-known methods.

a) X-ray scan: "X-ray security imaging is widely used to inspect luggage, mail, and vehicles. Currently, one line of development of X-ray security scanners is the adoption of multi-view systems that allow building a detailed 3-D structure of the scanned object." [1]

- Pros: The X-ray scan operates in a higher frequency range than our design. Thus, the resolution is higher than our project.
- Cons: The X-ray system is bulkier than our design. Since the frequency range of X ray is higher than 120GHz, the distance travelling of the wave is short. Thus, it is harder to detect objects from far away.

b) Ultrasound scan: "Ultrasound scanning is used in many medical settings to image and identify target anatomical structures, especially in soft tissue as it provides the required contrast to distinguish different tissues for diagnostic and therapeutic purposes." [2]

- Pros: The Ultrasound scan operates at higher frequency than our design. Thus, the resolution is better. In addition, ultrasound is used widely for biomedical imaging.
- Cons: The ultrasound wave cannot travel as far as our design. The range is between a few centimeters up to several meters.

c) Millimeter-wave scanning: “In this study, we investigate a millimeter wave (mmWave) synthetic aperture radar (SAR) imaging scheme utilizing a low-cost frequency modulated continuous wave (FMCW) radar to take part in non-destructive testing which could be a useful tool for both civilian and military demands.” [3]

- Pros: The development of the mmWave is growing. It covers a large field of application.
- Cons: The frequency of millimeter-wave is lower, so the resolution is lower.

4.6 Design Decisions

List key design decisions (at least three) that you have made or will need to make in relation to your proposed solution. These can include, but are not limited to, materials, subsystems, physical components, sensors/chips/devices, physical layout, features, etc.

- One of the key design decisions we made for the proposed solution is to create a web application to serve as our GUI instead of a downloaded executable program. To do this, we had to add a Raspberry Pi to the design to host the web application. This is to improve usability by not making the user download software to use the sensor and make it available to be viewed by multiple users at once.
- We decided to use a differential, 2 channel ADC. The decision is made based on the differential outputs of Radar IC. The voltage logic level is 3.3V, the same as the logic level of the FPGA.
- A programmable amplifier will be used for the buffer at the inputs of the ADC. The amplifier has different inputs and outputs.
- We decided to use the Alchitry Au FPGA to interface between the PC and Hardware components. This decision was made to increase speed as the previous solution was using a Data Acquisition Card which was working but very slowly. We decided to use the FPGA because we can streamline all the functionality for this specific use and hope to greatly increase speed on commands and data gathering.

4.7 Proposed Design

Discuss what you have done so far – what have you tried/implemented/tested?

- For Design 0, we started with the block diagram for all the components and the layout of the GUI.

- For Design 1, we had our schematic and layout for the RF board.

- For Design 2, we had our schematic and layout for the ADC board.

4.7.1 Design 0 (Initial Design)

Design Visual and Description

Include a visual depiction of your current design. Different visual types may be relevant to different types of projects. You may include: a block diagram of individual components or subsystems and their interconnections, a circuit diagram, a sketch of physical components and their operation, etc.

Describe your current design, referencing the visual. This design description should be in sufficient detail that another team of engineers can look through it and implement it.

Justify each component in the design with respect to requirements.

Block Diagram:

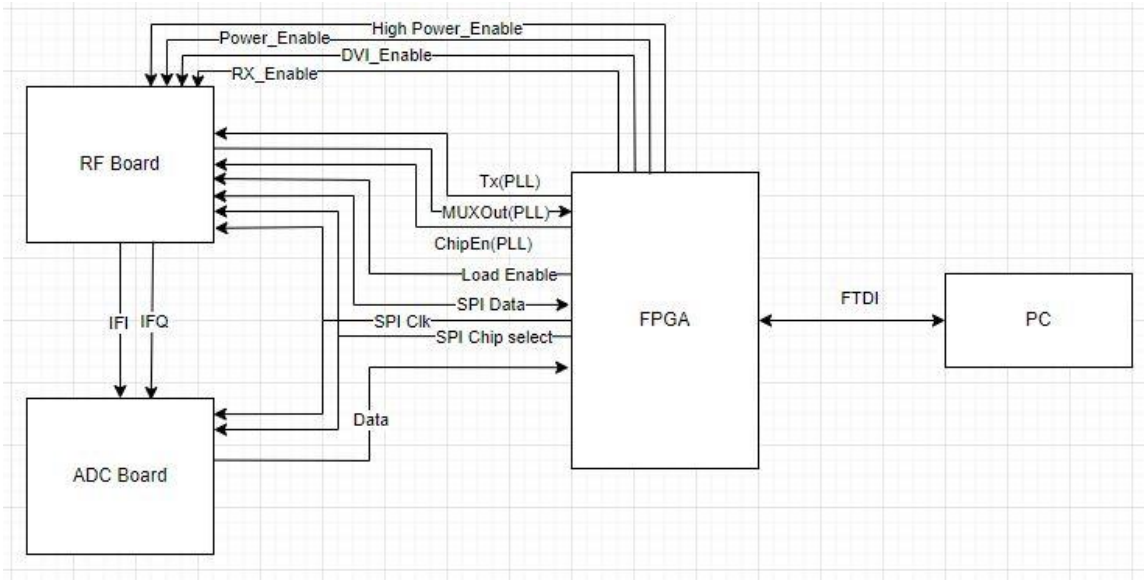

Figure 3: Project Block Diagram

The high-level diagram provides connections between different subsystems in the design. From the diagram, RF board outputs IFI and IFQ data to the ADC board for data sequencing. The ADC board will output the data to the FGPA. In addition, FPGA and RF board communicate through SPI lines. There are control pins of the RF board, such as High Power Enable, Power Enable, DVI Enable and RX Enable. They are controlled through programming the FPGA. The FPGA is connected to the PC through FTDI cables. The PC will process and display data.

Functionality

Describe how your design is intended to operate in its user and/or real-world context. This description can be supplemented by a visual, such as a timeline, storyboard, or sketch.

How well does the current design satisfy functional and non-functional requirements?

The sketch above provides all the functionalities required by the project. The RF board contains the radar IC and the Phase Lock Loop circuit that help the board emit the 120GHz frequency. The ADC board's functionality is to convert the analog IFI and IFQ data to digital data at 1MHz rate before the data is processed by the FPGA prior to the PC. PC helps with display and convert the raw data into the magnitude/ phase data.

4.7.2 Design 1 (Design Iteration)

Include another most matured design iteration details. Describe what led to this iteration and what are the major changes that were needed in Design 0.

There are no changes from design 0 in design 1. Design 1 provides more in-depth information on the RF board with different components. The RF board includes different components that comply the requirements of the project.

Design Visual and Description

Include a visual depiction of this design as well highlighting changes from Design 0. Describe these changes in detail. Justify them with respect to requirements.

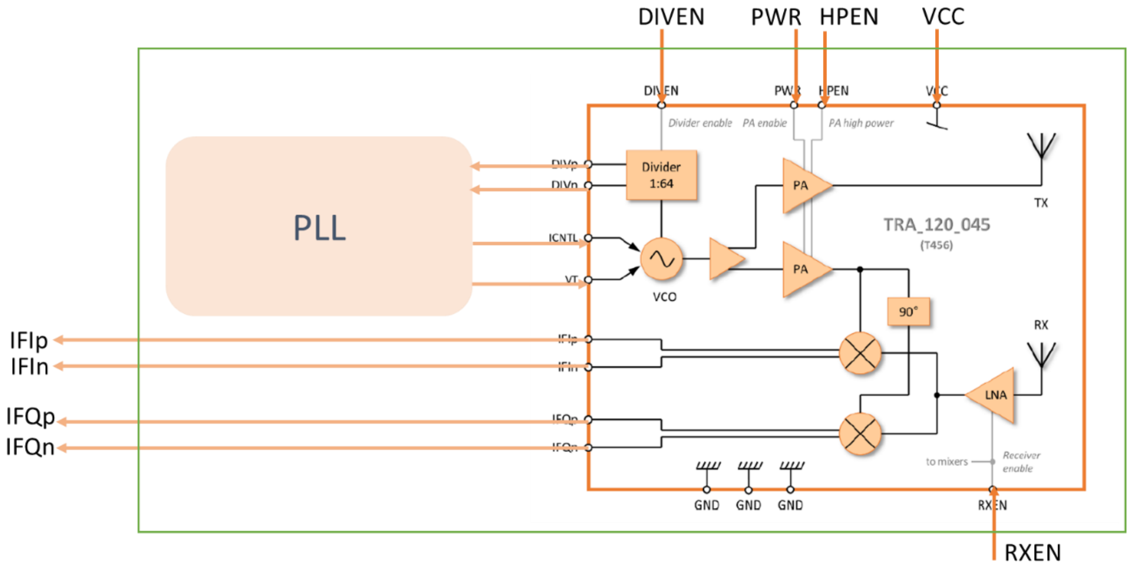

Figure 4: RF Board Design

The design includes two major parts: Phase Lock Loop circuitry and Radar IC. The radar IC is the component that emits the signal at 120GHz, and the phase lock loop circuitry helps with locking the right frequency for the IC.

4.8 Technology Considerations

Highlight the strengths, weaknesses, and trade-offs made in technology available.

Discuss possible solutions and design alternatives.

Strength of the technology: Frequency range of the system is high and wide band (center frequency of 120GHz and the detecting distance range is from 15 to 20 m. The processing time is fast (around 5ms). The size of the system is small.

Weaknesses and Tradeoff: The complication of using the FPGA for fast processing time. The system is expensive for limited uses (conducting imaging and object detection). The system is not easy to debug if there are problems with operation.

4.9 Design Analysis

- *Did your proposed design from 4.7 work? Why or why not?*
- *What are your observations, thoughts, and ideas to modify or iterate further over the design?*

Our proposed design from 4.7 works because the design composes of different subsystems that fulfill different requirements of the project: RF subsystem is responsible for emitting the right frequency or frequency range, ADC is responsible for data acquisition to be sent to the FPGA, FPGA is responsible for data processing time, and GUI is for user interaction. Those subsystems can be designed and tested separately for functionality before integration.

5 Testing

*Testing is an **extremely** important component of most projects, whether it involves a circuit, a process, power system, or software.*

The testing plan should connect the requirements and the design to the adopting test strategy and instruments. In this overarching introduction, given an overview of the testing strategy. Emphasize any unique challenges to testing your system/design.

5.1 UNIT TESTING

What units are being tested? How? Tools?

1) RF Board Testing:

a) The board is powered up correctly:

- The main supply voltage for the board is 5.5V. The voltage into the TRA_120_045 (the Radar IC) is designed to be 3.3V. The voltages into the ADF4159 (the PLL IC) include AVDD (3.3V) and DVDD/ SD_VDD (1.8V).
- The total current flows into the board should not exceed 1.25 A (the maximum current handling by the fuse).

b) The PLL can be programmed through FTDI cables locked at a frequency. To know whether the PLL is locked at a frequency. The MUXOUT pin allows various signals to be accessed internally, including the lock signal. In addition, the spectrum analyzer can be used to detect the frequency output from the radar IC.

c) The PLL can be programmed to sweep a certain range of frequency. The spectrum analyzer is used to detect the range of frequency.

2) ADC Board Testing:

a) The board is powered up correctly: There are supply voltages for MAX11192 (ADC), which are AVDD 5V and OVDD 3.3V. The amplifier is supplied by the VCC of 5V. Those voltage lines come from the FPGA's Header.

b) To test the functionality of the board, a voltage sine wave is sent to the ADC board. The raw ADC data is read from the FPGA and is reconstructed manually. If the reconstructed voltage value and waveform is the same as the original voltage sine wave, the ADC board passes the unit test.

3) FPGA Testing:

a) FPGA is programmed to communicate with the RF board or with the ADC board exclusively when it is specified by the operator.

b) FPGA can receive the voltage data (from sub section 2 above) and the user can access the raw ADC data.

4) User Interface Testing:

a) To test the data display functionality, we use a set of random generated data (IFI and IFQ) to input into the UI for display. There are several options for display, such as magnitude/ phase for IFI, IFQ and processed data for IFI and IFQ. If the UI can display the data based on the choice, the UI passes the data display functionality.

b) To test the control functionality, the simple test would be sending a command to blink the LED from the UI and to see if the LED on the Alchitry blinks or not.

5) Lens Modeling:

a) The lens is printed in 3D and used with the RF board. The far field signals from the lens are then recorded and measured to compare with the datasheet.

5.2 Interface Testing

What are the interfaces in your design? Discuss how the composition of two or more units (interfaces) are being tested. Tools?

There are several interfaces in the system, which varies from one sub system to the other.

Interfaces in the system includes:

- RF board to the PFGA (FPGA to the RF board)
- ADC board to the FPGA (FPGA to the ADC board)
- FPGA to the User Interface (User Interface to the FPGA)

To test the FPGA to the UI display interface, we will examine the user display output (raw ADC) based on the data that comes from the FPGA with the data is received directly from the ADC and RF boards. If the raw ADC data displayed on the UI (based on data coming from the FPGA) is the same as the data directly from the ADC and RF subsystem, the interface test from FPGA and User Interface is completed.

To test the interface between the RF board and the FPGA, we should be able to program the PLL (ADF4159) to lock at a certain frequency. The spectrum analyzer can be used to detect the output frequency of the board.

5.3 Integration Testing

What are the critical integration paths in your design? Justification for criticality may come from your requirements. How will they be tested? Tools?

a) The RF board emits signal at a desired frequency (120GHz) and receives the signal reflecting from objects. It then transmits the data (IFI and IFQ) data to the ADC board. The RF board contains two ICs (TRA_045 and ADF4159) that communicate with FPGA through SPI lines. Two ICs are programmed through SPI line based on the desired functionality and the user input from the UI. There are numerous tests that must be run as it performs different functions. The most important test is to measure the actual signal output with the actual emitted frequency. The test will determine whether the subsystem works correctly or not.

b) The ADC board receives data from the RF board and does data acquisition before passing the data to the FPGA for processing and display. Completion of ADC PCB integration requires that we test the accuracy of the analog-to- digital converted data from the ADC, which then passed to the FPGA.

c) The FPGA sends user-input commands from the UI (PC) to the RF board. In addition, it also receives data from the ADC PCB. The FPGA requires a large amount of embedded software, so it will require some standard software testing, including the SPI communication between the FPGA to the ICs on the RF board and ADC board and data transmit from the ADC board and to the PC. The test requires manual testing of the signals and commands being sent to and from those sub-systems, respectively.

d) The UI is used to send control signals and to display data. The UI is tested based on the software programming standard. There is manual testing to verify all the functions in the software working properly.

5.4 System Testing

Describe system level testing strategy. What set of unit tests, interface tests, and integration tests suffice for system level testing? This should be closely tied to the requirements. Tools?

a) RF PCB Design:
- Testing for interoperability with the FPGA.
- Testing for interoperability with the ADC board.
- Testing to ensure the phase locked loop (PLL) produces 2GHz signal.
- Testing to ensure the Radar IC (TRA_045) to emit 120GHz signal.
- Testing to ensure the data is transmitted from the RF board to the ADC board.

b) ADC PCB Design:
- Testing for interoperability with the FPGA (accurate transmission of digital signal from processing).
- Testing for interoperability with the RF board (accurate reception and conversion of analog signal).
- Testing to ensure ADC PCB sampling rate is 1MHz.
- Testing to ensure that the maximum frequency of data coming to the ADC IC is less than 500 kHz (Nyquist).
- Testing to ensure the ADC resolution is 16-bit.

c) FPGA Programming:
- Testing for interoperability with user ADC PCB (receiving digital signals)
- Testing for interoperability with RF PCB (sending operator commands)
- Testing for interoperability with the PC (User Interface, sending the data and receiving operator commands)

d) User Interface:
- Testing for interoperability with FPGA (sending the operator commands and receiving the data)
- Testing for the sufficient user satisfaction and intuitiveness (~80%)

5.5 Regression Testing

How are you ensuring that any new additions do not break the old functionality? What implemented critical features do you need to ensure do not break? Is it driven by requirements? Tools?

Regression testing is important in our system, as there are connections between different subsystems. Each sub-system will be introduced slowly and tested incrementally to stave off regression during all integration phases. For example, we will test the RF subsystem first and then the ADC subsystem with the FPGA before integrating the RF – ADC – FPGA together. The one-by-one subsystem introduction will allow our group to indicate which subsystem is malfunctioning.

5.6 Acceptance Testing

How will you demonstrate that the design requirements, both functional and non-functional, are being met? How would you involve your client in the acceptance testing?
We will detect an object from a distance.

1. Manual object distance measurements: We will know what objects are placed and their position.
2. The radar imaging system will emit a frequency (120 GHz) signal, then receives the reflected signal. Through ADC and FPGA, the data will then be presented on the UI within 5ms. The data should be processed and given out the information on where the object is detected.
3. The UI should also receive the information on control command, such as the frequency, to send to the FPGA and then control the PLL.
4. Comparison: UI-output-to-manual-measurement – This is the final and most important step. We will compare our initial manual measurement results to measurement results gleaned from the system-generated user interface plot/ result.

We will discuss an acceptable level of measurement error tolerance with our client. Preliminarily, we would like to produce distance detection/ measurements with no more than approximately 20% measurement error. In addition, the processing time should be no more than 5ms.

5.7 Security Testing (if applicable)

5.8 Results

What are the results of your testing? How do they ensure compliance with the requirements? Include figures and tables to explain your testing process better. A summary narrative concluding that your design is as intended is useful.

a) We started testing the Phase Lock Loop circuitry on our RF board. The PLL IC on the board receives 50MHz reference signal from the Crystal on board. The divider factor for the reference signal in the PLL is programmed to be 2. Thus, the output R-divider signal of the PLL IC should be 25MHz. The test is to verify that the PLL can be programmed based on desired specifications. Using the Spectrum Analyzer, we detected that the R-divider signal was 25 MHz, as expected.

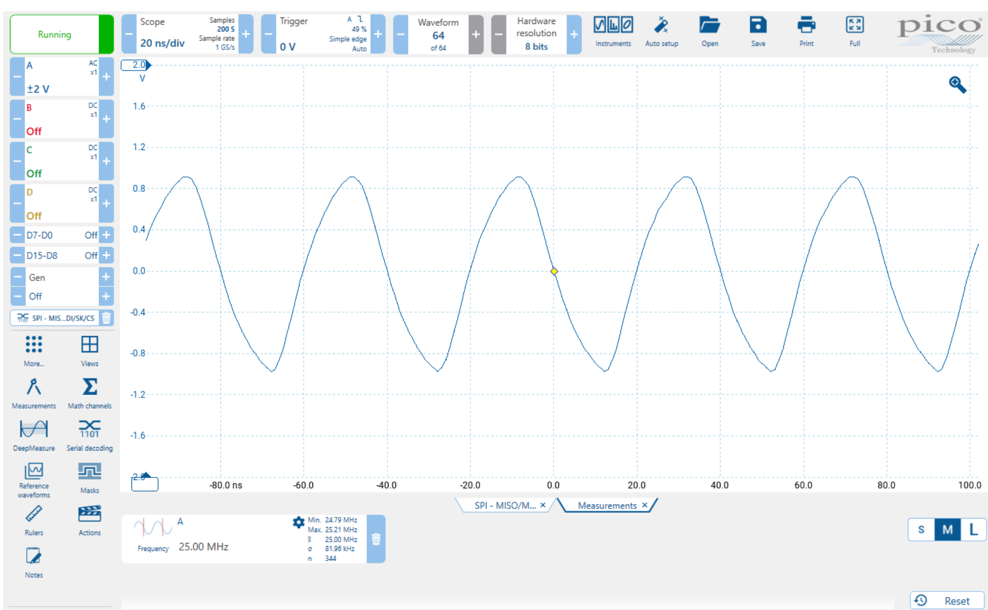

Figure 5: The R-divider signal of the PLL

b) The PLL is programmed to set the emitting frequency of the Radar IC to be 120GHz. Thus, the Div-n and Div-p outputs of the Radar IC should have the frequency of 1.875 GHz. We used the spectrum analyzer to probe Div-n and Div-p outputs, and we got 1.875 GHz as expected. This confirms that our RF board can emit 120 GHz frequency.

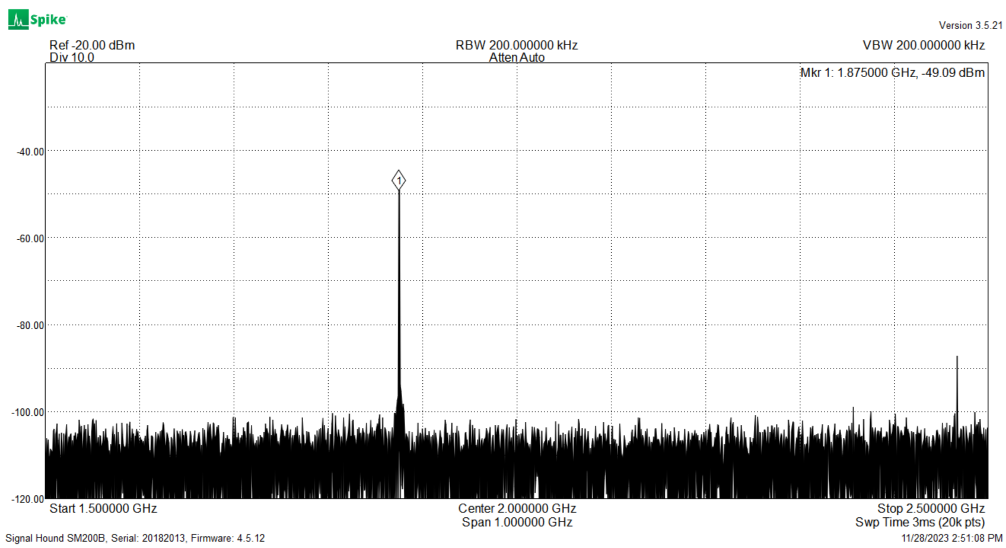

Figure 6: Div - p result of 1.875 GHz

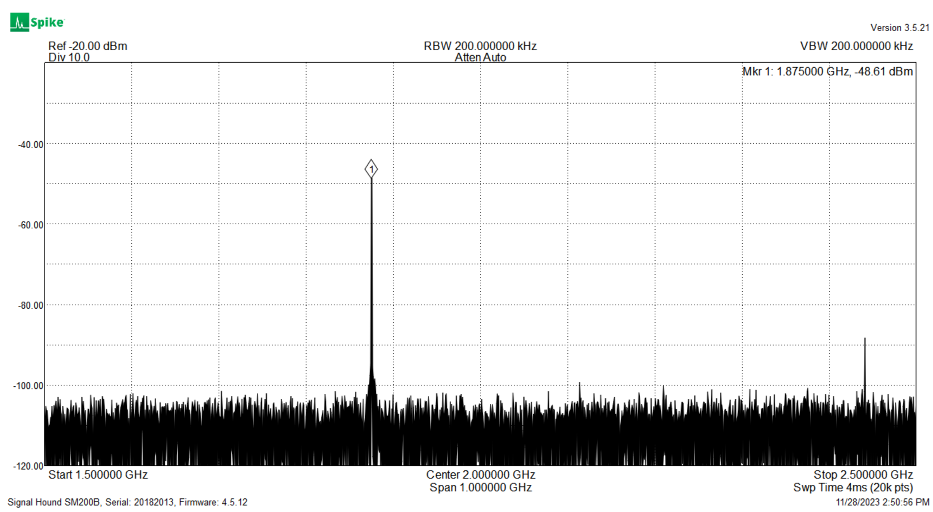

Figure 7: Div -n result of 1.875 GHz

6 Implementation

Describe any (preliminary) implementation plan for the next semester for your proposed design in 3.3. If your project has inseparable activities between design and implementation, you can list them either in the Design section or this section.

Our implementation plan for the next semester includes:

a) Test Measurements for frequency sweep of the RF board using in the Spectrum Analyzer: We conduct a test to check the output of the RF board when sweeping the frequency, like what we did for a single frequency.
b) Test the operation of the ADC board for the correct analog to digital conversion.
c) Test the embedded program of the FPGA to communicate with the ADC board for data and RF and ADC board for control signal.
d) Test the embedded program of the FPGA to communicate with the PC.
e) Implement the system to do object detection.
f) Implement the system to do imaging.

7 Professionalism

This discussion is with respect to the paper titled "Contextualizing Professionalism in Capstone Projects Using the IDEALS Professional Responsibility Assessment", *International Journal of Engineering Education* Vol. 28, No. 2, pp. 416–424, 2012.

7.1 Areas of Responsibility

Pick one of IEEE, ACM, or SE code of ethics. Add a column to Table 1 from the paper corresponding to the society-specific code of ethics selected above. State how it addresses each of the areas of seven professional responsibilities in the table. Briefly describe each entry added to the table in your own words. How does the IEEE, ACM, or SE code of ethics differ from the NSPE version for each area?

The table includes a copy of table 1 from the paper "Contextualizing Professionalism in Capstone Projects Using the IDEALS Professional Responsibility Assessment", *International Journal of Engineering Education* Vol. 28, No. 2, pp. 416–424, 2012" and a copy of the IEEE code of Ethics and a column of differences discussion.

Area of Responsibility	NSPEE Definition	NSPE Canon(s)	IEEE Canon(s)	Comparison
Work Competence	Perform work of high quality, integrity, timeliness, and professional competence.	Perform services only in areas of their competences. Avoid deceptive acts.	"6. to maintain and improve our technical competence and to undertake technological tasks for others only if qualified by training or experience, or after full disclosure of pertinent limitations;" "9. to avoid injuring others, their property, reputation, or employment by false or malicious action;" "10. to assist colleagues and co-workers in their professional development	The NSPE definition and canon are rather precise, whereas the IEEE code of ethics elaborates on falsification and malicious action. The IEEE code of ethics also lists a responsibility to mentoring coworkers to aid in their professional development, and this is not discussed in the NSPE table.

			and to support them in following this code of ethics."	
Financial Responsibility	Deliver products and services of realizable value and at reasonable costs.	Act for each employer or client as faithful agents or Trustees.	"2. To avoid real or perceived conflicts of interest whenever possible, and to disclose them to affected parties when they do exist;" "4. To reject bribery in all its form;"	The IEEE code of ethics specifically lists conflicts of interest which are often financial in nature whereas the NSPE definition and canon are a bit vaguer.
Communication Honesty	Report works truthfully, without deception, and understandable to stakeholders.	Issue public statements only in an objective and truthful manner. Avoid deceptive acts.	"3. To be honest and realistic in stating claims or estimates based on available data;"	The IEEE and NSPE statements are quite similar in meaning and content.
Health, Safety, Well-Being	Minimize risks to safety, health, and well-being of stakeholders.	Hold paramount to the safety, health, and welfare of the public.	"I, to accept responsibility in making decisions consistent with the safety, health, and welfare of the public, and to disclose promptly factors that might endanger the public or the environment;"	Both the IEEE and NSPE codes of ethics use nearly identical language. The IEEE has more elaboration.
Property Ownership	Respect property, ideas, and information of clients and others.	Act for each employer or client as faithful agents or Trustees.	"7. to seek, accept, and offer honest criticism of technical work, to acknowledge and correct errors, and to credit properly the contributions of others;"	Both of these code sections from both papers describe ideas as property.
Sustainability	Protect environment and natural resources locally and globally.	(None provided)	"1. to accept responsibility in making decisions consistent with the safety, health, and welfare of the public, and to disclose promptly factors that might endanger the public or the environment;"	Both codes of ethics (IEEE and NSPE) clearly state that engineers have a responsibility to preserving the welfare of the environment. The IEEE code does not explicitly list the necessity to preserve natural resources.

Social Responsibility	Produce products and services that benefit society and communities.	Conduct themselves honorably, responsibly, ethically, and lawfully so as to enhance the honor, reputation, and usefulness of the profession.	“5. to improve the understanding of technology; its appropriate application, and potential consequences;” “8. to treat fairly all persons and to not engage in acts of discrimination based on race, religion, gender, disability, age, national origin, sexual orientation, gender identity, or gender expression;”	The NSPE code does not touch on the need to Avoid discrimination based on various social issues. categorizations, like in #8 of the IEEE code.

7.2 Project Specific Professional Responsibility Areas

For each of the professional responsibility areas in Table 1, discuss whether it applies in your project’s professional context. Why yes or why not? How well is your team performing (High, Medium, Low, N/A) in each of the seven areas of professional responsibility, again in the context of your project? Justify.

Area of Responsibility	Application in the Project	Performance Rating
Work Competence	Each of the team members in the project needs to be responsible for their tasks. The failure in doing such can result in the failure of the whole project, since our design contains a lot of subsystems,	High
Financial Responsibility	Not Applicable because our system is small and not too expensive.	N/A
Communication Honesty	We need to communicate honestly with each other in working to understand each other’s work and progress. We need to present our project honestly to our advisor for any help or advice and to our client.	High
Health, Safety, Well-Being	We need to make sure that our project works as intended to	High

	provide the best outcomes for users.	
Property Ownership	Not applicable because we are responsible for any confidential information.	N/A
Sustainability	Not applicable because the product is not in mass production and does not contain any hazardous materials.	N/A
Social Responsibility	We want to keep in mind what are the usages of the products to make the product better.	High

7.3 Most Applicable Professional Responsibility Area

Work competence is the most applicable area because it demonstrates our ability as an engineer. As the project depends on so many smaller subsystems and different expertise. We need each of the team members to be responsible and competent in their work.

7 Closing Material

7.1 Discussion

Discuss the main results of your project – for a product discuss if the requirements are met, for experiments-oriented project – what are the results of the experiment, if you were validating a hypothesis – did it work?

Requirements:

- Design RF circuit that contains radar IC and phased-lock-loop (PLL) circuitry.
- Design data acquisition (including amplifier, low pass filter, and ADC) and control circuitry with FPGA.
- Program FPGA to interface to ADCs for data collection from RF circuit.
- Program a USB chip to interface to a PC for data transfer.
- Program a GUI on the PC to interface to the FPGA.
- Conduct radar imaging experiments in the microwave lab at CNDE.

We have finished the first and the second requirements. For the RF PCB, we have tested, and the PCB has met two of the test requirements (PLL IC is operational, and the radar emits a frequency of 120 GHz. We finished the design of the ADC PCB. We need to test the board to know if it meets the requirements.

7.2 Conclusion

Summarize the work you have done so far. Briefly reiterate your goals. Then, reiterate the best plan of action (or solution) to achieving your goals. What constrained you from achieving these goals (if something did)? What could be done differently in a future design/implementation iteration to achieve these goals?

In summary, we have finished the first and second milestones (designing the RF and ADC board). In addition, we have tested the RF board. We started on learning the FPGA programming and on programming the GUI.

In the next semester, we will mainly focus on the programming aspects of the project. We need to have the FPGA communicating to the ADC and RF board for control signal, to receive data from the ADC board, and to communicate with the PC. We also need the GUI to be workable.

7.3 References

List technical references and related work / market survey references. Do professional citation style (ex. IEEE).

[1] BitRefineHeads, "Deep Learning X-ray," BitRefineHeads, 2023. [Online]. Available: https://heads.bitrefine.group/use-cases/object-recognition/116-object-recognition/298-deep-learning-x-ray. [Accessed 21 October 2023].

[2] A. F. Al-Battal, I. R. Lerman and T. Q. Nguyen, "Object Detection and Tracking in Ultrasound Scans Using an Optical Flow and Semantic Segmentation Framework Based on Convolutional Neural Networks," in ICASSP 2022 - 2022 IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP), Singapore, Singapore, 2022.

[3] T.-H. Pham, K.-H. Kim and I.-P. Hong, "A Study on Millimeter Wave SAR Imaging for Non-Destructive Testing of Rebar in Reinforced Concrete," Sensors, 2022.

7.4 Appendices

Any additional information that would be helpful to the evaluation of your design document.

If you have any large graphs, tables, or similar data that do not directly pertain to the problem but help support it, include it here. This would also be a good area to include hardware/software manuals used. May include CAD files, circuit schematics, layout etc., PCB testing issues etc., Software bugs etc.

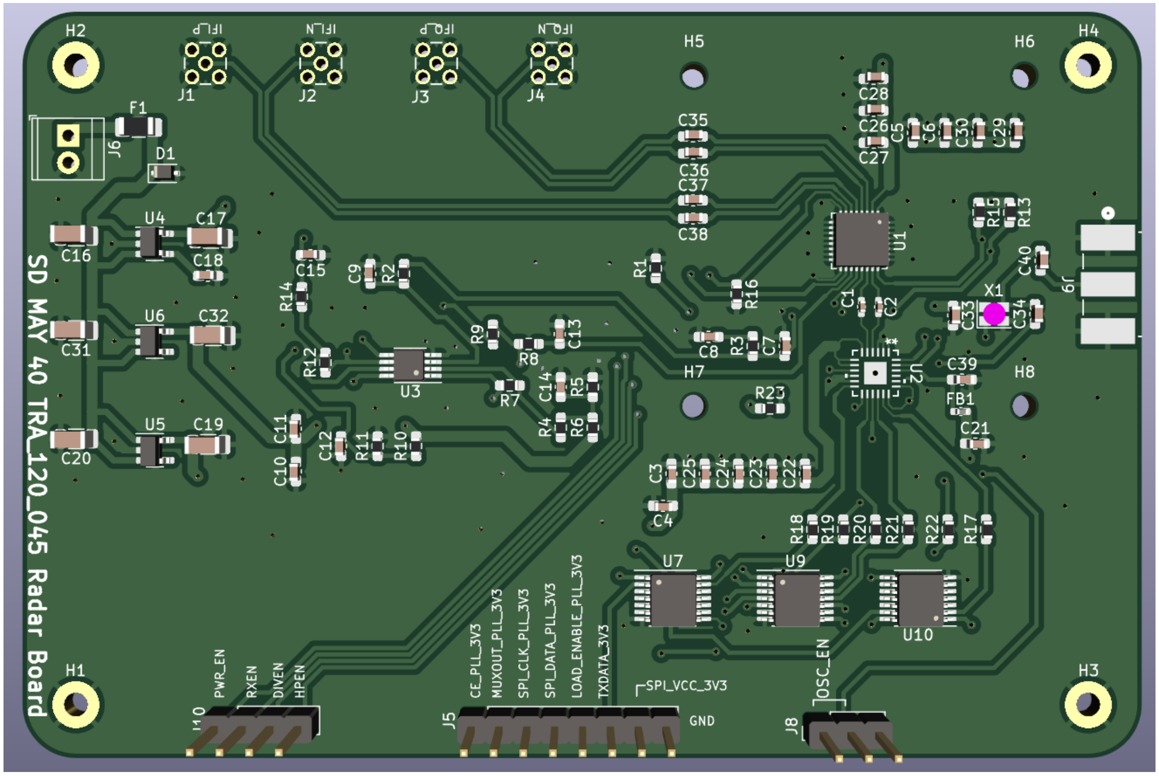

Figure 8: RF Board Layout

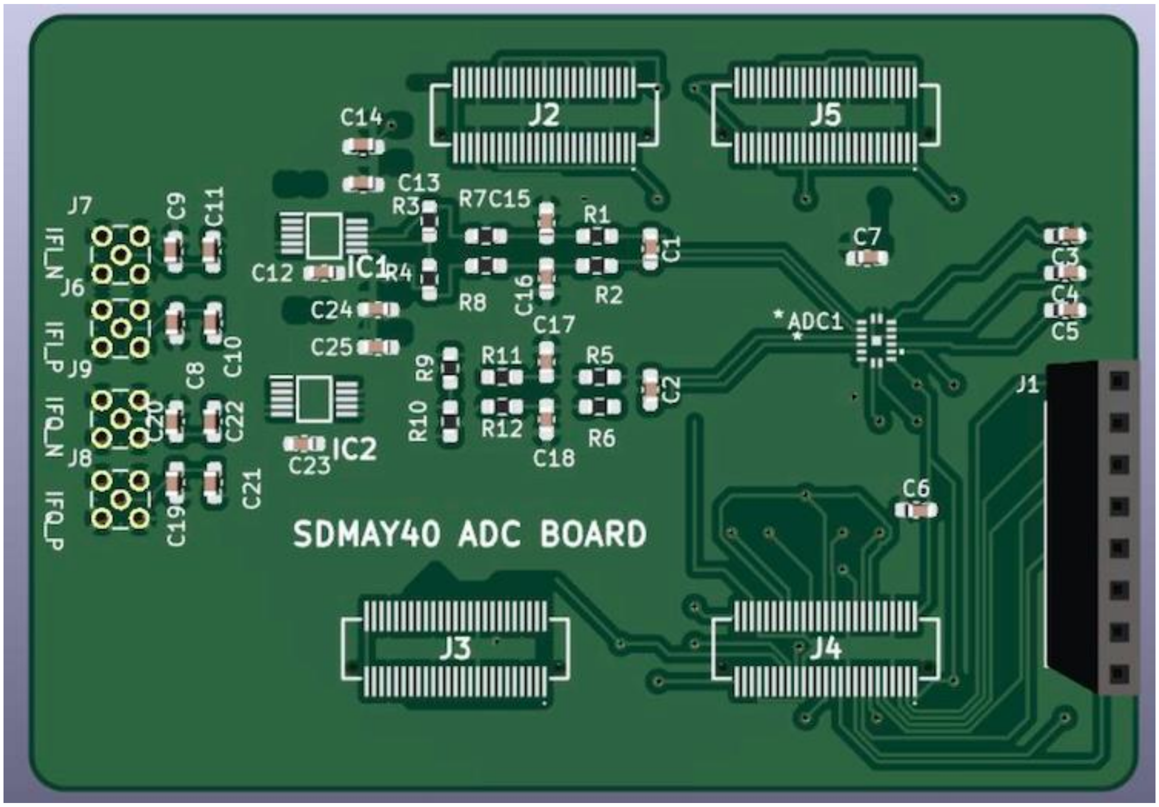

Figure 9: ADC Board Layout

7.4.1 Team Contract

Team Members:

1) Aaron D McCarville

2) Huyen Vy Pham

3) Noah Gaffney

4) Gunnar Hageman

5) Benjamin Podjenski

Team Procedures

1. Day, time, and location (face-to-face or virtual) for regular team meetings:

Type: Face to Face Meeting

Location: Applied Science Complex II (1915 Scholl Road) Rm 118

Time: Every Wednesday from 12:15 pm to 1 pm

2. Preferred method of communication updates, reminders, issues, and scheduling (e.g., e-mail, phone, app, face-to-face):

Git for project issues. Urgent matters use email, or text.

3. Decision-making policy (e.g., consensus, majority vote): Consensus
4. Procedures for record keeping (i.e., who will keep meeting minutes, how will minutes be shared/archived):

Upload to Git wiki immediately afterwards and keep everyone updated.

The minute is updated by Vy and uploaded on the Cybox.

Participation Expectations

1. Expected individual attendance, punctuality, and participation at all team meetings:
- Expected to attend, barring unforeseen circumstances.
- Please let our team know if you are going to miss the meeting in advance.
- Expect to read the meeting minutes afterward and work on the assigned tasks.

2. Expected level of responsibility for fulfilling team assignments, timelines, and deadlines:
- Make sure assignments are done on time and communicate early on if deadline needs to be pushed back.
- Communication on late completion should be done at least 24 hours in advance. Please update on the issue any work in the progress.

3. Expected level of communication with other team members:
- Frequent communication. Use git prolifically to tack project issues and progress.

4. Expected level of commitment to team decisions and tasks:
- Very high.

Leadership

1. Leadership roles for each team member (e.g., team organization, client interaction, individual component design, testing, etc.): Vy: team organization.

The rest will be split equally among everyone, including Vy.

2. Strategies for supporting and guiding the work of all team members: Use Git issues. Comment on the issue and tag the person you need help with (if known). Otherwise, bringing the issue up in the meeting too.
3. Strategies for recognizing the contributions of all team members:

Git issues will track this. Close the issue when you are done. Mention what you did in the weekly meeting.

Collaboration and Inclusion

1. Describe the skills, expertise, and unique perspectives each team member brings to the team.

Vy: PCB design, C, MATLAB, Python, RF measurement

Aaron: Xilinx FPGA's, USB, KiCad, Python, C, C++, RF measurement

Noah: KiCad, C, PCB design, circuit assembly

Gunnar: Python, C, Java, Armature Radio background, project management/design doc work.

Ben: Java, C, Python, .NET, systems engineering experience

2. Strategies for encouraging and support contributions and ideas from all team members:

Be respectful and listen to everyone when discussing problems. Be ready to help if you can.

3. Procedures for identifying and resolving collaboration or inclusion issues (e.g., how will a team member inform the team that the team environment is obstructing their opportunity or ability to contribute?)

Bringing up the problems to the person before bringing up to the team. When you decide to bring up the collaboration and inclusion issues to the team, the issue will be discussed among team members. The solutions will be proposed by everyone and finalized by consensus. If you feel like the problem is not resolved after applying the solution, please bring up to the advisor with a head-up for other team members.

Goal setting, Planning, and Execution

1. Team goals for this semester:

Produce functional radar (hardware and software, including GUI).

2. Strategies for planning and assigning individual and teamwork:

Assigning milestones and small tasks on Git. The second milestone should be decided in the middle or near the end of the first milestone. Issues are created under milestones and are designed for work for a week. The start of an issue is the weekly meeting day, and the end is a day prior to the following meeting day. The work will be discussed in the weekly meeting to make sure everyone is up to date with the project's progress.

3. Strategies for keeping on task:

Tracking issue on Git. Provide a quick summary and upload files (if have) on the git issue before closing. The summary and any files of work will be used to check the work.

Consequences for Not Adhering to Team Contract

1. How will you handle infractions of any of the obligations of this team contract?

Bring up the infractions in the meeting. Discuss as a team and make a decision based on consensus.

2. What will your team do if the infractions continue?

Bring it up to the advisor and decide whether they should stay in the team.

****

a) *I participated in formulating the standards, roles, and procedures as stated in this contract.*

b) *I understand that I am obligated to abide by these terms and conditions.*

c) *I understand that if I do not abide by these terms and conditions, I will suffer the consequences as stated in this contract.*

1) Huyen Vy Pham DATE: 09/07/2023

2) Aaron McCarville DATE: 09/08/2023

3) Benjamin Podjenski DATE: 09/08/2023

4) Noah Gaffney DATE 09/08/2023

5) Gunnar Hageman DATE 09/08/2023